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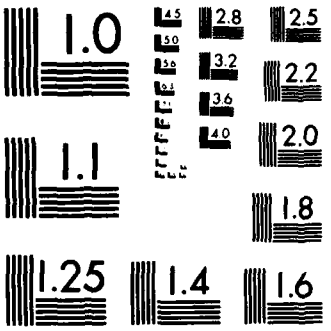
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ANNUAL REPORT

Research in VLSI Reliability

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Objective

In order to increase the circuit density and speed of VLSI systems, microelectronic device geometry is shrinking from a few microns to submicron and beyond. This scaling has greatly heightened the need for a better understanding of the failure mechanisms affecting the long-term reliability of VLSI system and for improved methods of designing and testing for reliability. In contrast to production technologies and circuit performances, whose failures to meet specifications will be either obvious or relatively easily discovered before the circuits are incorporated into complex systems or missions, reliability failures cannot be easily or completely eliminated. When they do occur, reliability failures can be costly in many ways.

The objective of this research is to gain basic scientific understanding of the mechanisms of the three leading hard failure modes: oxide wearout, hot-electron-induced degradations, and contact and metal failures. The basic understanding should lead to failure models and methods to improve reliability assurance through design, processing, and testing techniques.

Approach and Progress

I. Thin Oxide Reliability

Extensive experimental studies have been performed on the two leading MOSFET oxide reliability limits: time-dependent dielectric breakdown and charge trapping. We have found that oxide breakdown is due to hole generation in the oxide by energetic electrons that are injected into the oxide through Fowler Nordheim tunneling. (The exact mechanism of hole generation is not yet clearly understood.) Some of the holes are trapped in the oxide causing an increase in the cathode field and hence an increase in the electron current density which leads to increased hole generation rate. This positive feedback eventually causes breakdown.

A significant consequence of this understanding is an improved method for extrapolating the time-to-breakdown, t_{BD}, measured at high oxide field, E_{ox}, to obtain the oxide lifetime at a much lower operating field. $\ln(t_{BD})$ should be extrapolated as a linear function of $1/E_{ox}$ rather than E_{ox} as in the current practice. Improvement in lifetime estimate by order(s) of magnitude may be expected.

Breakdown, of course, occurs at localized weak areas, where the feedback gain is higher due to reduced oxide thickness or large local hole trap density, etc. We have shown that the defect (weak area) density as a function of the degree of weakness can be characterized by simple time-to-breakdown measurements. Using this information we proved experimentally that the oxide lifetime and failure rate can be predicted for any circuit size and electric field. Furthermore, this technique can predict the effect of and optimize the electrical screen procedure. The conclusion of this improved scientific understanding of oxide reliability is that reliable oxides can be produced at much thinner thicknesses than hitherto considered possible. Or, at a given oxide thickness, failure rate can be reduced by two orders of magnitude by optimizing the screen procedure.

Ion-beam damage of the silicon dioxide has long been an issue of concern in integrated circuit industry. In MOS fabrication processes and space applications, the silicon dioxide layer is often exposed to ion bombardment. The residual oxide damage caused by the ion bombardment can be annealed out at temperatures around 500°C without any apparent degradation of the threshold voltage. However, reliability of these devices after prolonged usage is an issue that needs to be addressed.

We have used constant-voltage stressing to study the interface states generation and charge trapping in Si implanted polysilicon/SiO_2/Si system after high temperature annealing at 950°C. After the annealing, no observable surface charge existed at the Si/ SiO_2 interface for implant doses less than 2×10^{13} cm^{-2}. However, the residual of the implant induced damage was found to cause large interface states generation and enhance hole and

electron trapping. For equal number of injected electrons, the induced interface state density was found to increase with implant dose. The density of hole trapping centers was found to saturate at 3×10^{12} cm^{-2} for implant doses higher than 2×10^{12} cm^{-2}. The density of electron traps (N_0) increased monotonically with the implant dose. The trapping cross section of the implant induced electron trapping centers is about 1.6×10^{-20} cm^{-2}, which is much smaller compared with that of the unimplanted oxide (about 2×10^{-19}).

II. Hot-Carrier Induced Degradation

A common approach to studying the hot-electron-induced device degradation is to perform lengthy measurements of device degradation for a wide range of channel lengths and voltages and empirically determine the reliability bounds. Our research has shown that hot-electron-limited device lifetime is a unique function of the channel electric field and is therefore closely correlated with the substrate current, which is an easily measurable current flowing out of the substrate lead and is a result of the impact ionization events in the same channel electric field. Once the lifetime-substrate current relationship is determined, the lifetime of a specific device at specific bias voltages can be quickly determined by measuring the substrate current in that device at those bias voltages.

During a long stress test, however, the substrate current can vary significantly as charge builds up near the drain causing a change in the electric field. This introduces considerable error in the lifetime -- substrate current tests. We have developed a computer controlled test system that automatically adjusts the drain stressing voltage to keep the substrate current at a constant value. In another version, the gate voltage is also adjusted to keep $V_d - V_g$, hence the oxide field near the drain, constant. Using this "constant field" testing method we have studied the physics of device degradation.

The critical electron energy for damaging the interface is found to be 3 to 6 eV depending on the oxide field. These are 50% higher than previous reports. We have further identified interface trap generation with a role by hydrogen at the Si/ SiO_2 interface and electron trapping as two equally important mechanisms of device degradation. The microscopic events leading to the generation of interface traps and electron traps is one subject of our current research.

III. Failure Mechanisms of Electromigration with AC Pulses

The electromigration failure of Al thin film has been extensively studied under constant current conditions. Integrated circuits, however, often operate with uni-directional or bi-directional current pulse. Aside from vacancy relaxation, other differences exist between pulsed and continuous current stressing. Among them are the reduced average power dissipation in pulse powered conductor and possible temperature gradients along the conductor to promote thermal diffusion. These differences warrant the investigation of thermal effects on Al, Al/Si and alloyed Al conductors by pulsed current.

Design of an electromigration test station to perform pulsed current stressing on wafer level is near completion. Our setup has the capability to do 25 MHz pulsed tests with 10 ns current pulses of 4×10^6 A/ cm^2. The station will employ a personal computer to perform automated testing. The power supply, digital multimeter and the switching relay are all interfaced to the computer to perform simultaneous stressing and multiplexed measurement of many test structures.

Publications

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[3] J. Lee, I.C. Chen, S. Holland, Y. Fong, and C. Hu., "Oxide Defect Density, Failure Rate and Screen Yield," Digest of Technical Papers, VLSI Technology Symposium, May 1986, pp. 69-70.

[4] S. Holland, I.C. Chen, J. Lee, Y. Fong, K.K. Young, and C. Hu, (Invited Paper), "Time-Dependent Breakdown of Thin Oxides," to be published in Proceeding of Silicon Nitride and Silicon Dioxide Thin Insulating Film Symposium, October 1987.

[5] J.Y. Choi, P.K. Ko, and C. Hu, "Effect of Oxide Field on MOSFET Degradation," submitted to IEEE Trans. Electron Devices.

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